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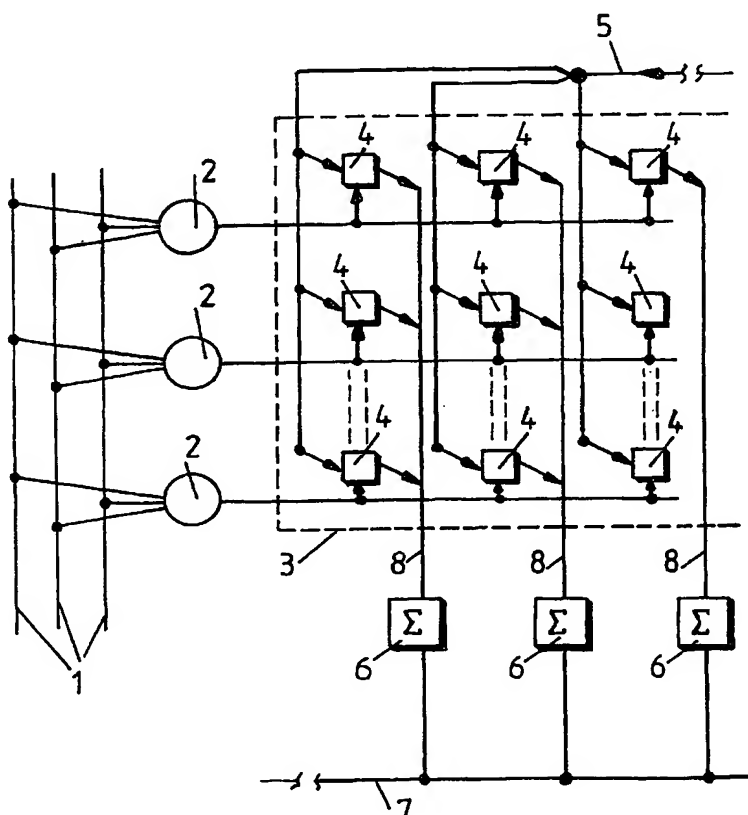
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(54) Title: **INEXACT ADDRESSABLE DIGITAL MEMORY**



(57) Abstract. A memory configuration for use in a computer system, the memory comprising a plurality of address decoders each of which is allocated an identifier having a predetermined number of bits, each bit having first and second selectable states, and a data memory having a plurality of word lines of predetermined length, each of the said address decoders being activatable to select one of the plurality of word lines, and the address decoders comprising means to receive an input address having a predetermined number of bits and means to compare the identifier of an address decoder with the input address wherein the memory further comprises means to activate an address decoder if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier.



TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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☐ Further documents are listed in the continuation of box C.

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8 document member of the same patent family

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